IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application: Duc Chau et al. Serial No.: 10/052,234 Filed: January 16, 2002 For: SELF-ALIGNED TRENCH MOSFETS AND METHODS FOR MAKING THE SAME	Confirmation No. 9589 Group Art Unit: 2823 Examiner: J. Garcia

Mail Stop Non-Final Response
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. §1.131

Sir:

We, the undersigned, declare that:

1. We are the inventors of the subject matter in the above-captioned patent application;

2. We conceived of the invention disclosed and claimed in the above-captioned patent application and reduced that invention to practice prior to January 24, 2001.

3. Attached hereto as Exhibit A is a document evidencing the facts in paragraphs 1 and 2. Portions of that document that are not relevant to the present Declaration have been redacted.

4. That all statements are made of our own knowledge are true and all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such

willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

Duc Chau _____ Date

Becky Losee 1-13-05 Date

Bruce Marchant 1/13/05 Date

Dean Probst 1/13/05 Date

Robert Herrick 1/13/05 Date

James Murphy 1/13/05 Date

willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

[signature]	1/20/2005
Duc Chau	Date
Becky Losee	Date
Bruce Marchant	Date
Dean Probst	Date
Robert Herrick	Date
James Murphy	Date

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SEMICONDUCTOR TM

Invention Disclosure

DO NOT WRITE IN THIS SPACE

Assigned File No:NUMBER HERE

Date of receipt: *00/00/0000*By: *TYPE HERE*

Please complete each item of this form. If an item is not applicable, enter "N/A"

General Information Concerning the Invention

Title of invention: *Low cost, High Density Vertical Trench MOSFET Process*

Brief description of the invention:

Background - Section 1: MOSFET power devices require low RDSon achieved by adding a number of transistors in series. The closer the transistors are together (a higher density), then a less area on a wafer is needed. The higher density, in turn, reduces a cost of manufacturing the device.

A form of the transistors is a vertical transistor using a trench, allowing the vertical transistor to be made in three dimensions, greatly reducing the area needed on the wafer. The trench is etched into the wafer, then a gate oxide is grown on all sides of the trench. A gate conductor (10) (poly silicon) is placed in the trench. An isolation dielectric (4A) is placed over the conductor to electrically isolate the conductor from other conductive layers that will be placed on the wafer in later processing. Because this isolation dielectric must not be over a plurality of portions of the device, a masking step (22) is used to define the portions where the dielectric must not be present and then the dielectric is etched in that portion. Because an alignment tolerance (6) is needed (the alignment tolerance is the amount of over-sizing needed to compensate for variations in alignment), the density of the transistors is reduced, making the cost of manufacturing higher.

An oxidation of a Silicon surface occurs when the Silicon surface is exposed to Oxygen. This oxidation of the Silicon surface is referred to as growing an oxide. A high temperature accelerates the oxidation of the Silicon surface, hence, the growth of the oxide. The presence of a water atmosphere also enhances this growth of the oxide. Nitride (16) blocks the growth of the oxide by inhibiting the Oxygen from reaching the Silicon surface. The grown oxide would electically isolate the poly silicon gate conductor from the other conductive layers that will be placed on the wafer in later processing.

Doping oxides with various chemicals will change the rate at which the oxide will etch with a given etching procedure. This doping also changes the reflow characteristics of the oxide. For example, increasing the amount of Phosphorous in the oxide will increase the etch rate for Hydroflouric Acid wet etches, while adding Boron will decrease the etch rate for the same etch.

Phosphorous doping will also cause the oxide to flow more readily at high temperatures, which will make the surface nearly planer.

A selective depositing system will deposit an oxide onto silicon and oxide, but will not deposit oxide onto Nitride.

Spin on Glass (SOG) is a planerizing dielectric that is dripped onto a wafer, the wafer is spun using surface tension of the SOG to spread it over the surface. The SOG is then cured by a temperature anneal.

Invention -

Key Features:

7 to 8 masks process with passivation

Recess Poly etch to ~0.50□m

Striped source mask design

No body contact mask: Blanket heavy body implant

Planer contact design

The differences involved in this process include:

1. Self-aligned isolation dielectric which allows the trench transistors to be made closer together by eliminating the alignment tolerance necessary for a separate mask. (Note, this alignment tolerance can be reduced by the purchase of expensive, new alignment tools, but could never match the density allowed by elimination of this alignment tolerance.)

2. All of the self-alignment process proposals would planerize the trenches, making step coverage by the metal easier and providing a good planer surface for wire bonding or bump placement.

3. The striped source mask allows the elimination of the heavy body implant mask and grounds the body, preventing snap-back without an additional mask.

This process with striped source and planer contact design, the vertical trench MOSFET cell pitch will reduced to sub-micro width which result in cell density per area increases exponentially. This will improve performance of the power MOSFET dramatically in terms of RDSon and current drive. Invention includes the process and design of ultra high-density vertical trench MOSFET and technique of grounding the channel to prevent snap-back and turning on the parasitic bipolar transistor. The process eliminates critical alignment, which enables the design of sub-micron cell pitch; as a result cell density per area increases exponentially. This results in high current drive and low on-resistance. By using a self aligned isolation dielectric(4C), the alignment tolerance is not required, thus allowing for the higher density of the transistors, reducing the cost of manufacturing the device. As an added benefit, the self-aligned isolation dielectrics greatly reduce the topography that must be covered adequately in later processing.

There are at least 4 ways of manufacturing the isolation dielectric for the self-aligned process:

I. The method of manufacturing the self-aligned dual-doped isolation dielectric comprises the steps:

a) Etching a conductor (10) in trench lower than a surface of the wafer.

b) Covering the entire wafer with a slow-etch dielectric (7) doped so the etching of this dielectric is slow.

c) Covering the slow-etch dielectric (7) with a fast-etch dielectric (5) doped so the etching of this fast-etch dielectric is faster than the slow-etch dielectric and the dielectric will reflow more readily than that of the slow-etch dielectric.

d) Reflowing both the slow-etch dielectric and the fast-etch dielectric (the dielectrics) so the surface of the fast-etch dielectric is uniform, showing none to little topography from the trench (Figure 3).

e) Etching the dielectrics to the point where the dielectrics are removed from the portions of the wafer where the dielectrics must not be present, while leaving the slow-etch dielectric in the top of the trench. This adequately electrically isolates the conductor in the trench from any other non-isolating layers, which may be used in the manufacturing of the device and also planerizes the surface.(Figure 4)

Note: Another variation would be to only place one type of dielectric, reflow and etch; leaving an isolation dielectric in the trench, because it would be thicker in the trench than out of the trench.

II. Growing an oxide (the dielectric) on the conductor which, in this case, must be poly silicon comprising the steps:

a) Using a nitride (16) layer to mask (protect) a part of a wafer where a purality of trenches will not be etched;

b) Etching the trenches;

c) Growing a gate oxide in the trenches;

d) Depositing the poly silicon;

e) Removing an excess poly silicon from the surface of the wafer insuring the poly silicon in the trenches is etched below the surface;

f) Growing an isolation dielectric oxide layer in a high temperature oxidation furnace and

g) Removing the nitride, leaving the isolation dielectric oxide to isolate the conductor from any non-insulator layers that follow in a manufacturing process.

III. Using a selective dielectric deposit system that will only deposit the dielectric on silicon exposed surfaces comprising the steps:

a) Using the nitride layer to mask (protect) the part of the wafer where the trenches will not be etched;

b) Etching the trenches;

c) Growing a gate oxide on the sides of the trench;

d) Depositing poly silicon over the surface of the wafer;

e) Etching the poly silicon in the trench lower than the surface of the wafer using a mask to protect the poly silicon outside the trenches where it is desired to have the poly silicon remain;

d) Selectively depositing the dielectric on the exposed poly silicon; and

e) Removing the nitride, leaving the oxide to isolate the conductor from any non-insulator layers that follow in the manufacturing process.

IV. Using a SOG (Spin on Glass) process comprising the steps:

a) Etching the conductor in trench lower than a surface of the wafer;

b) Using well-established procedures, applying the SOG in such a manner so the SOG only remains in the trenches and edges of the poly silicon on the field; and

c) Curing the SOG sufficiently so the conductor in the trench is electrically isolated from any other non-isolating layers, which may be used in the future steps in the manufacturing of the device.

In addition, using methods I or IV, elimination of the contact mask is also possible. Rather than following the SOG isolation dielectric process with a BPSG step to isolate the poly from the other conductive layers (usually metal) or the BPSG reflow with a mask, leave the poly, the body and the source of the transistors with no isolation oxide. Then use the metal mask to horizontally separate the gate from the source eliminating the

contact mask entirely. The metal will make contact with the poly on the field oxide for connection to the gate. The metal of the source will make contact to the body while being isolated from the trenches. The included figures show various layout options for horizonally isolating the source and the gate. (Please note that the figures are not to scale nor are they maximized for efficient layout, but are intended to demonstrate the invention only.)

Attach photocopies of all pertinent documentation. Each page must be signed, dated, and witnessed by two other persons who have read and understood the description of the invention.

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Description of Invention

Date of first description:

Date of first written description:

Date of first disclosure to others at Fairchild:

Construction and Testing of the Invention

Date of computer simulation:

Date of first prototype:

Date first prototype was tested to confirm desired operation of invention:

Attach date photocopy of results of testing of test pattern mask or first prototypes.

If the invention has been computer simulated attach a dated photocopy of this simulation.

Is the invention planned or used by Fairchild in a product or the method of manufacture or test of a product?

If yes, what is the part number and function? *N/A*

When will this Product utilizing their invention be available for sampling or "offered for sale"?

Related Art

Closest related art:

Publication, Sampling, or "Offer for Sale" of the Invention

Certain types of inventions, such as process steps or testing techniques, are typically used internally with Fairchild without outside persons becoming aware of the use. Such use may still be considered a commercialization, if the invention is being used to manufacture or test a product for purposes beyond mere engineering evaluation purposes.

Development Contract or Joint Development

Estimated Sales

Description and Drawing Illustrating the Invention

You must include drawings which illustrate the invention, including circuit schematics, structures, process steps, etc.

If you have original drawings in your lab notebook, please attach photocopies of the pertinent pages.

Execution of this Form

Witnessing of this Form

Submission of this Form

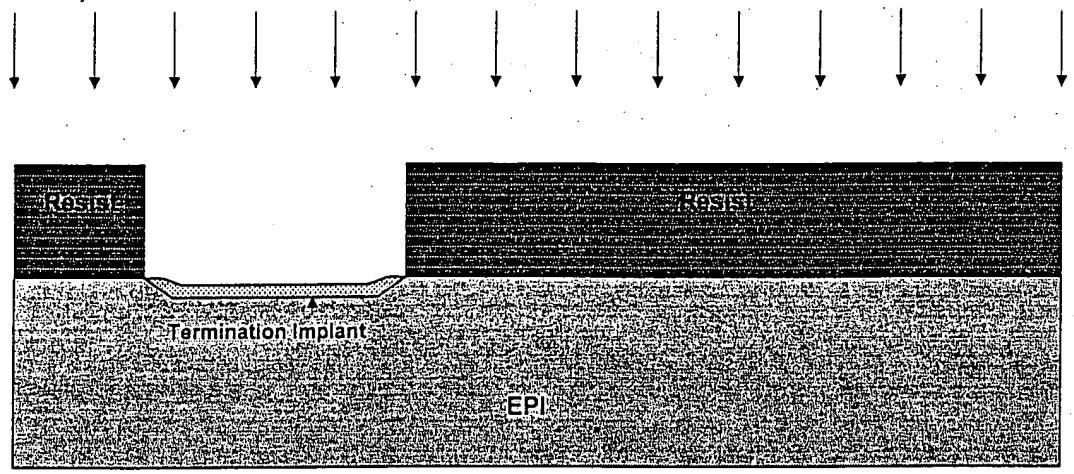
Please return the completed form, including your drawings, written description, photocopies of all pertinent pages from your engineering notebook (s), and other attachments, to Intellectual Property Group Patent Engineer responsible for your product group.

Process

EPI

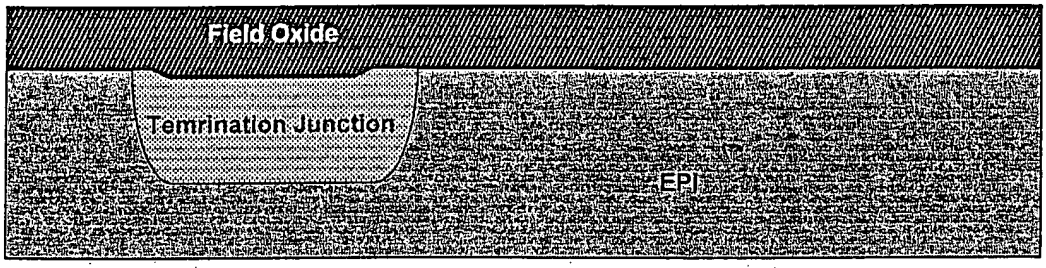
1st Termination Implant Mask

Termination Implant: 30-60keV, Boron 1E14-5E15



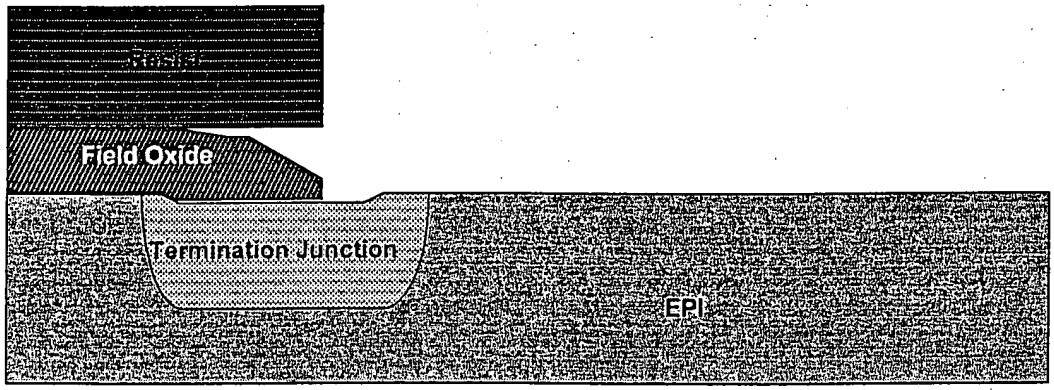
Resist Strip

Field Oxidation and drive: 1000°C-1100°C: 2kA-10kA

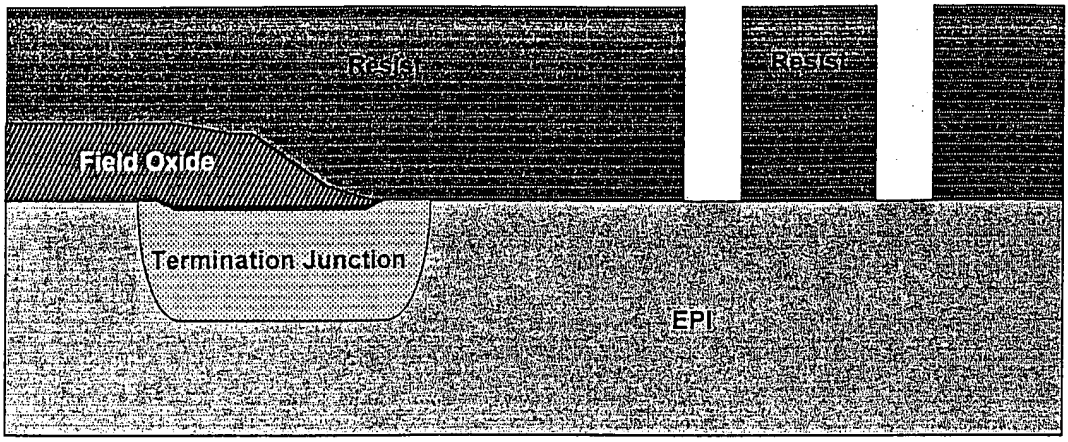


2nd Active Mask

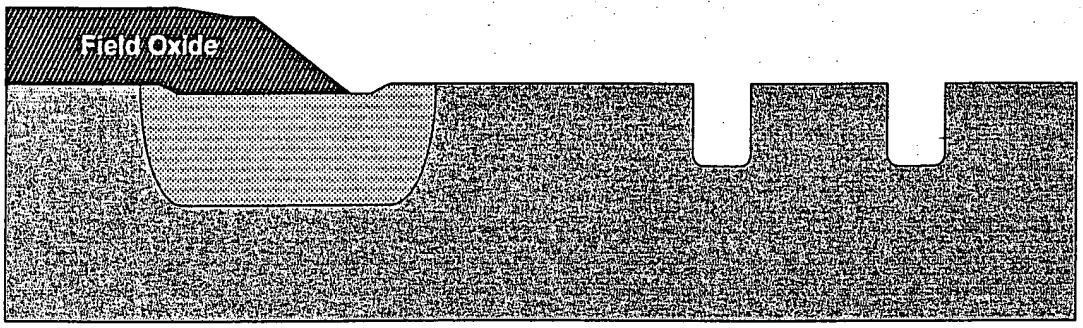
Active Etch



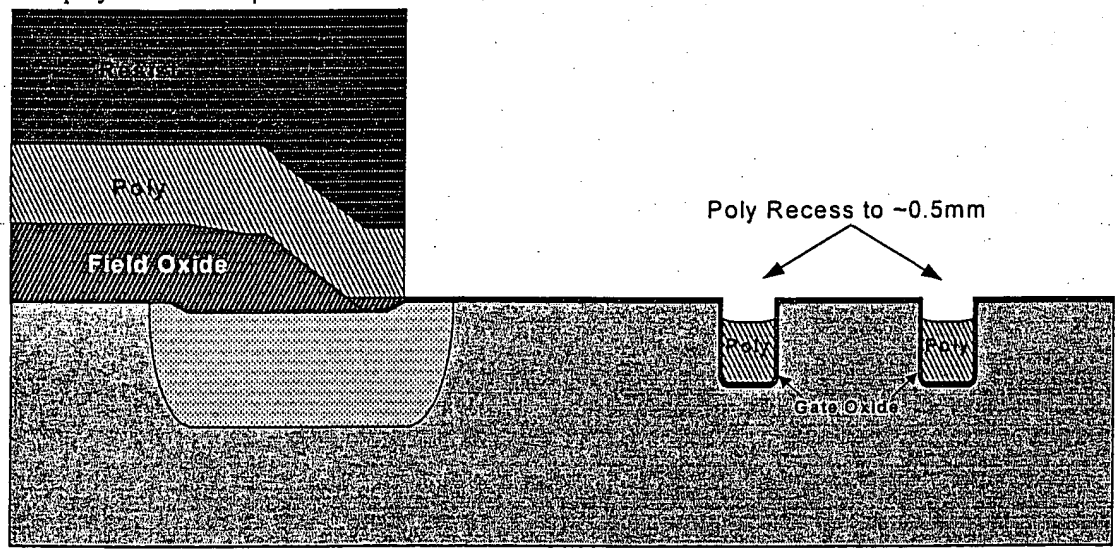
Resist Strip
3rd Trench Mask



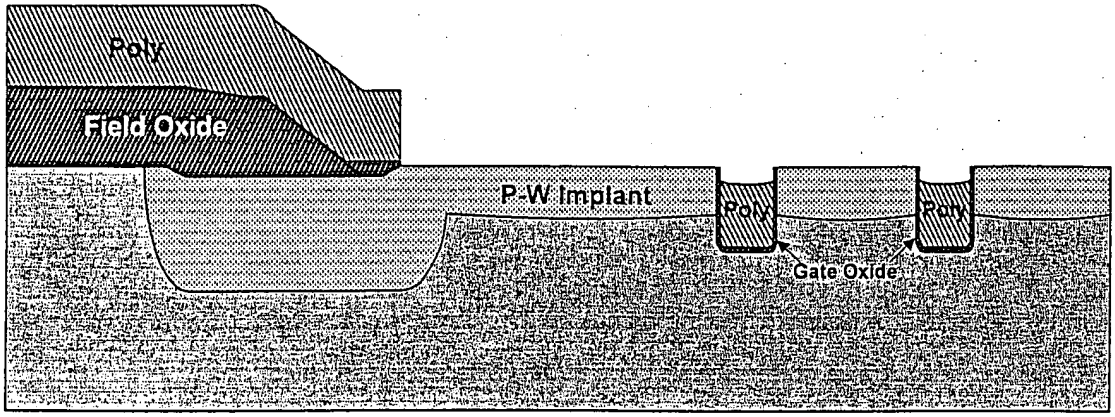
Silicon Trench Etch: 0.50 - 2.0μm
Resist Strip



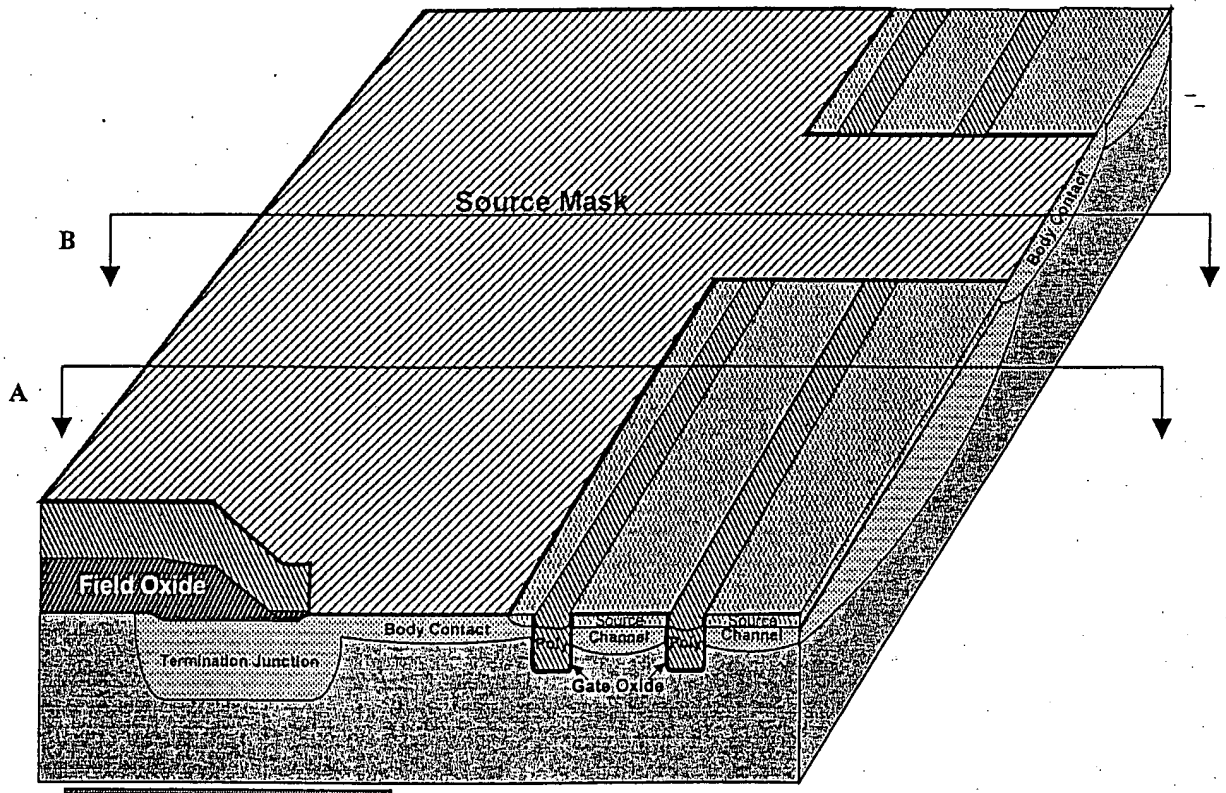
Gate Ox
Poly Deposition
Poly Dope
4th Poly Mask
Poly Etch – recess trench poly: 0.25 – 0.80μm

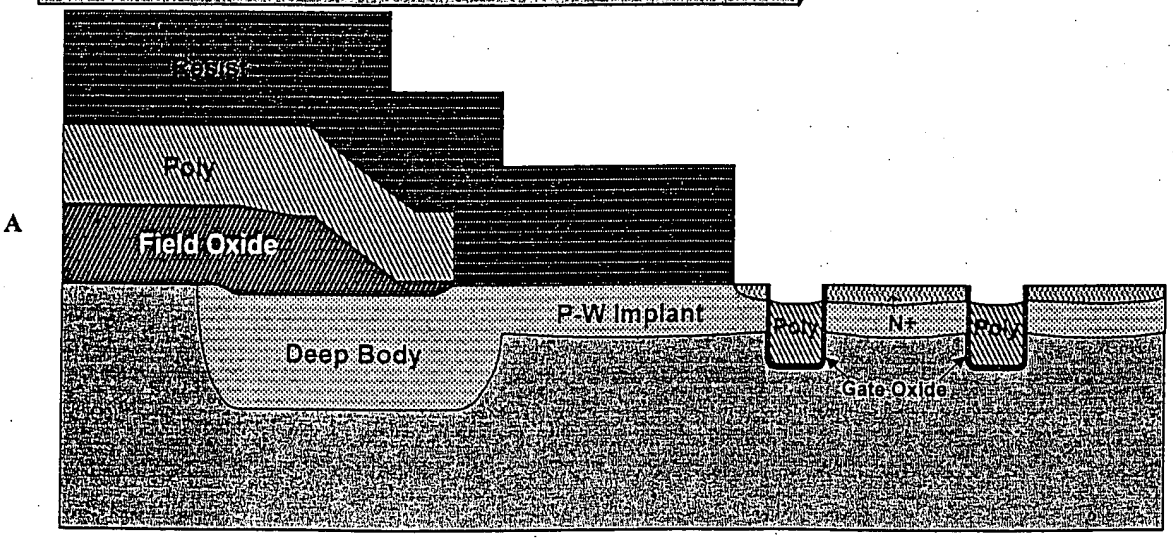


Resist Strip
Channel Implant 30keV-80keV Boron 3.0E
Channel Drive: ~1100C 20-60min

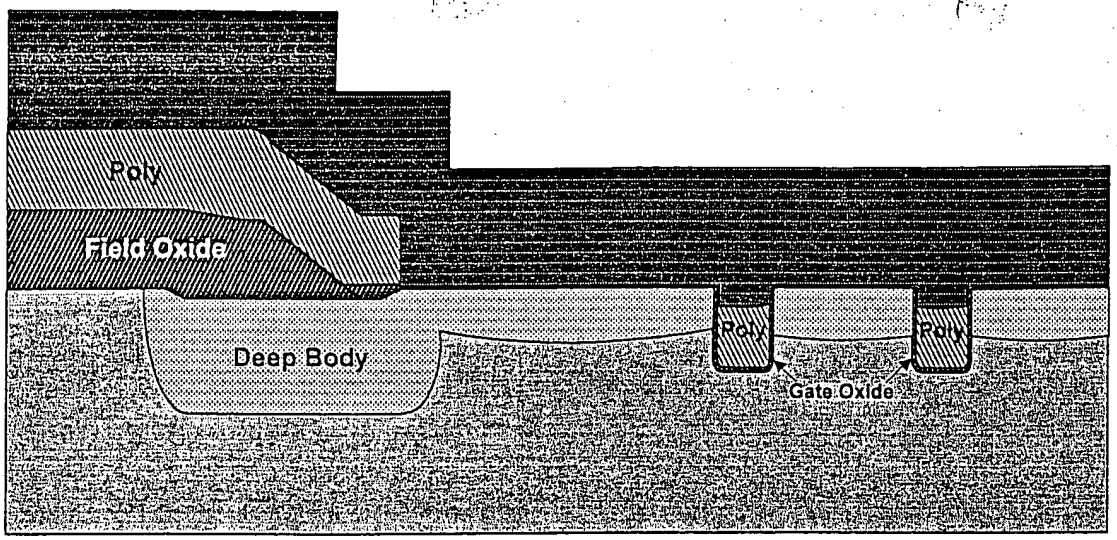


5th Striped Source Mask
Source Implant ~ 80keV As 8E15



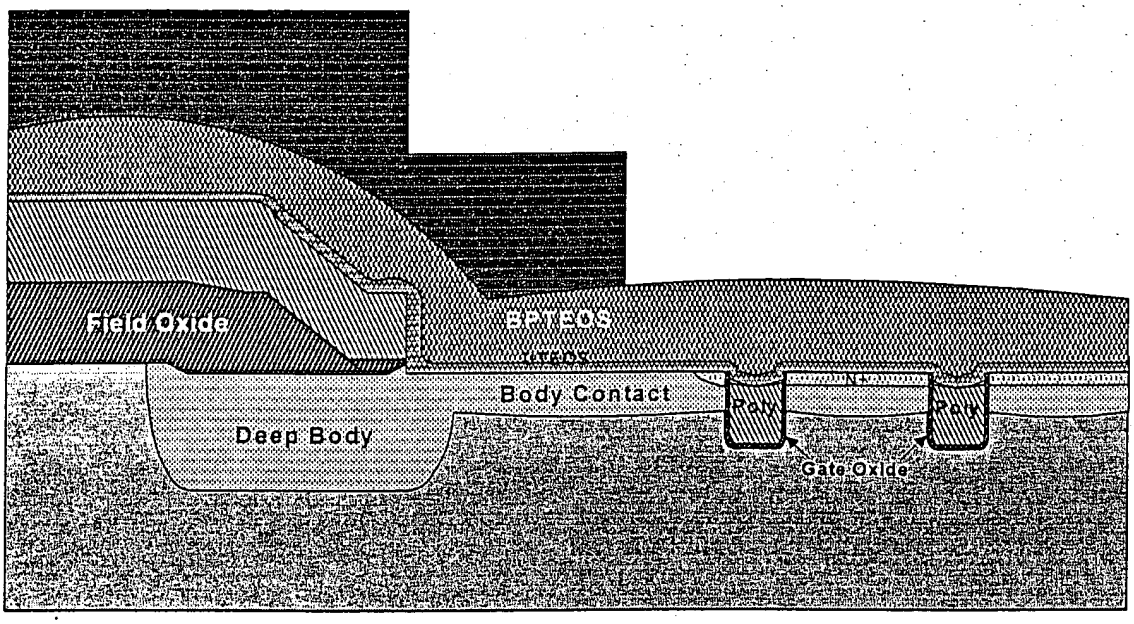


B

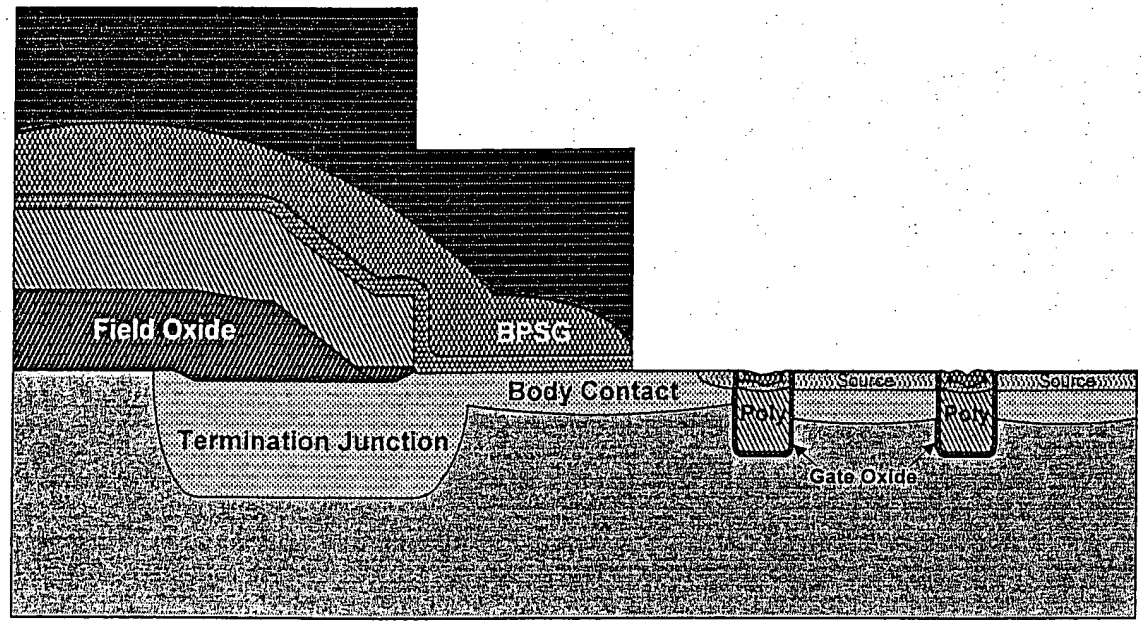


Resist Strip
N+ Drive: ~60min 850-950°C
Body Contact Implant: 40-100keV Boron: 8E14 – 2E15
Implant Anneal: RTA or Standard Furnace Anneal

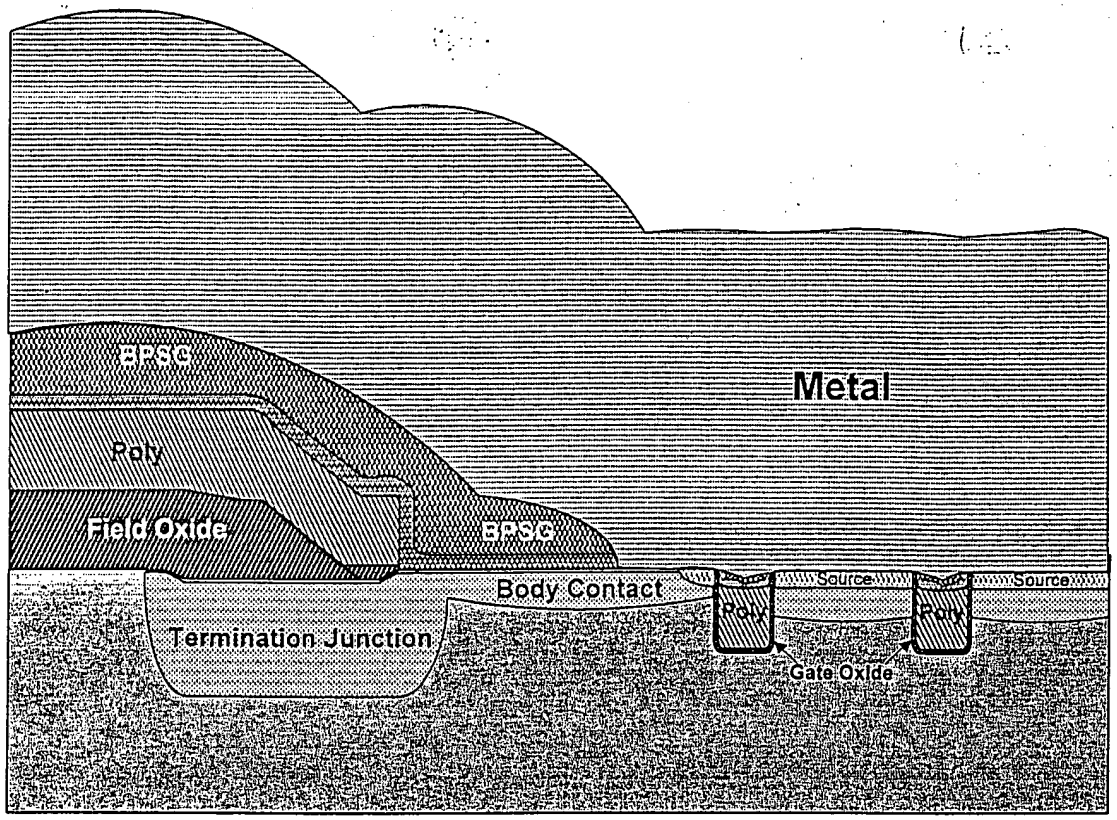
Dielectric Deposition: Un-doped Oxide and BPSG ~1kA°/4kA°
BPSG Flow: 800-950°C Dry O2 for ~30-60min.
6th Contact Mask



Contact Etch: Anisotropic Dry etch follow by BOE wet etch or uniform endpoint etch.



Resist Strip
Metal Dep. ~ 2.5μm – 10μm Al-Si
7th Metal Mask
Metal Etch
Resist Strip


Metal
BPSG
Poly
Field Oxide
BPSG
Body Contact
Source
Source
Poly
Poly
Termination Junction
Gate Oxide

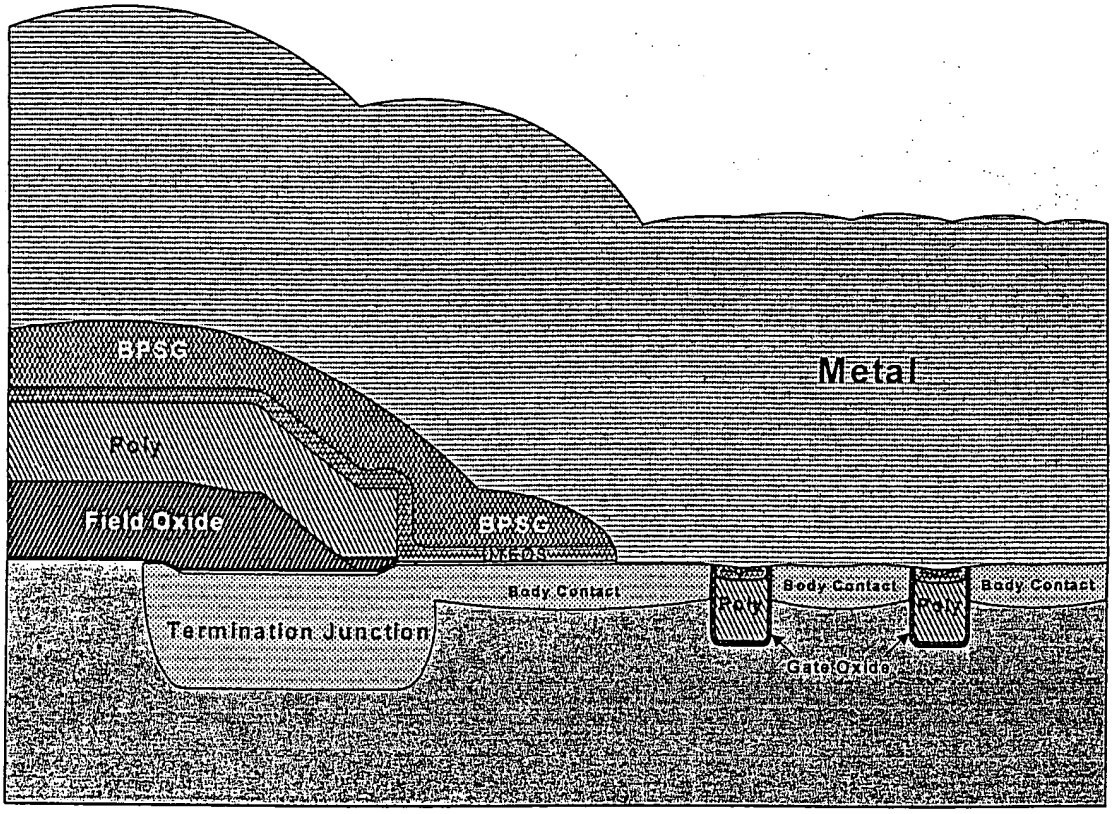

Metal
BPSG
Poly
Field Oxide
BPSG
Body Contact
Body Contact
Body Contact
Poly
Poly
Termination Junction
Gate Oxide

Figure 1 Standard process before etch

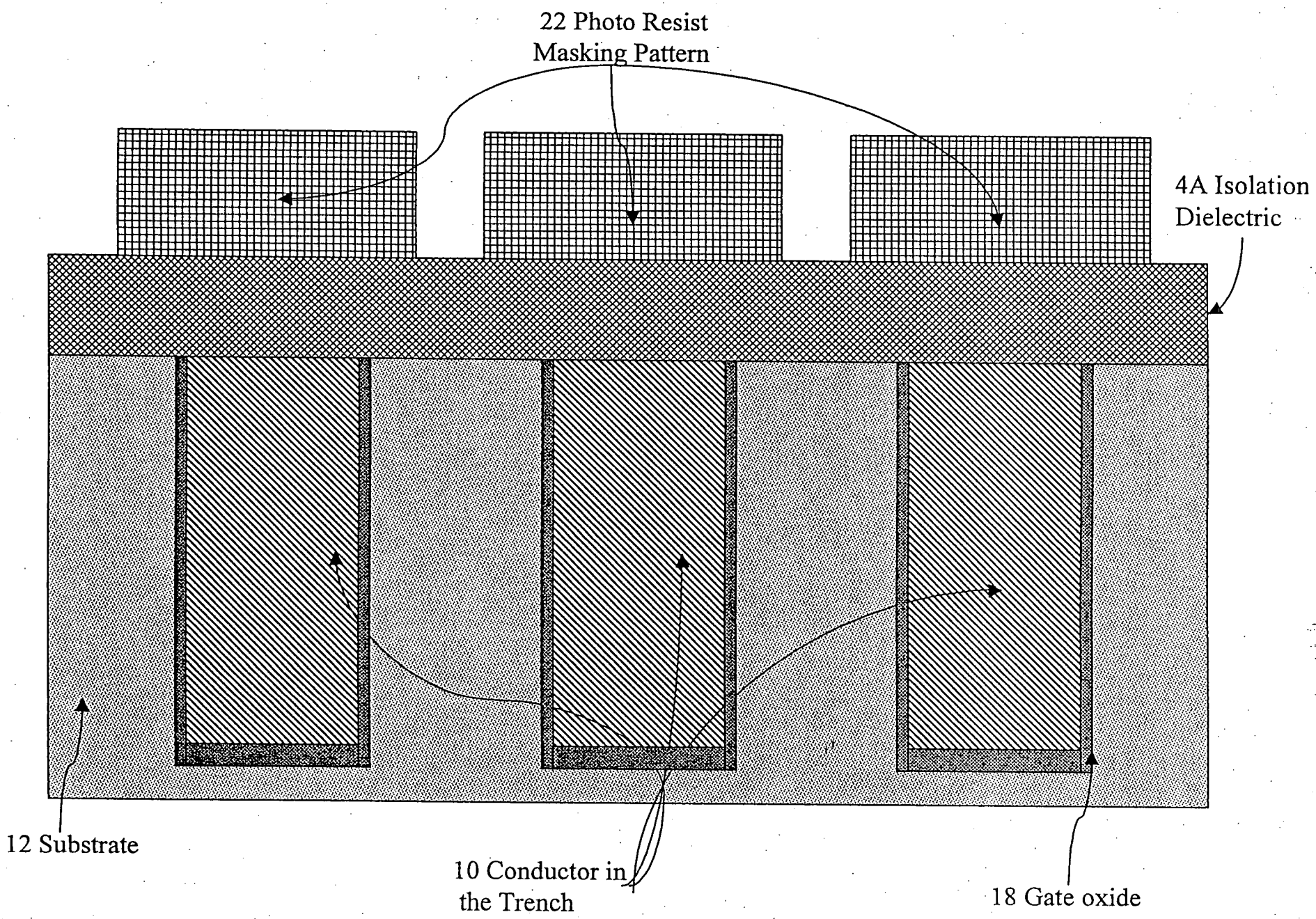


Figure 2 Standard process after etch

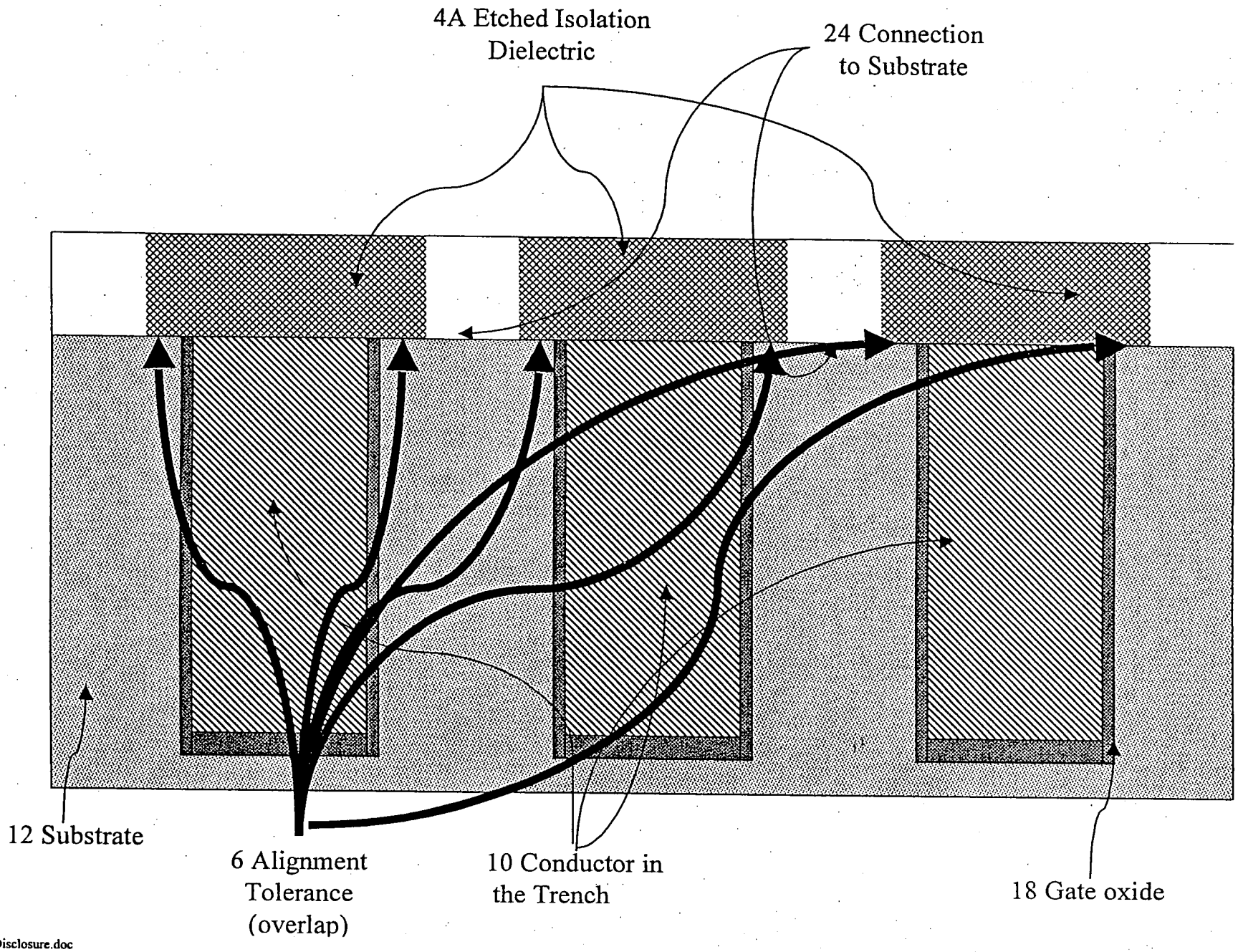


Figure 3 Dual Isolation Dielectric after reflow prior to etch

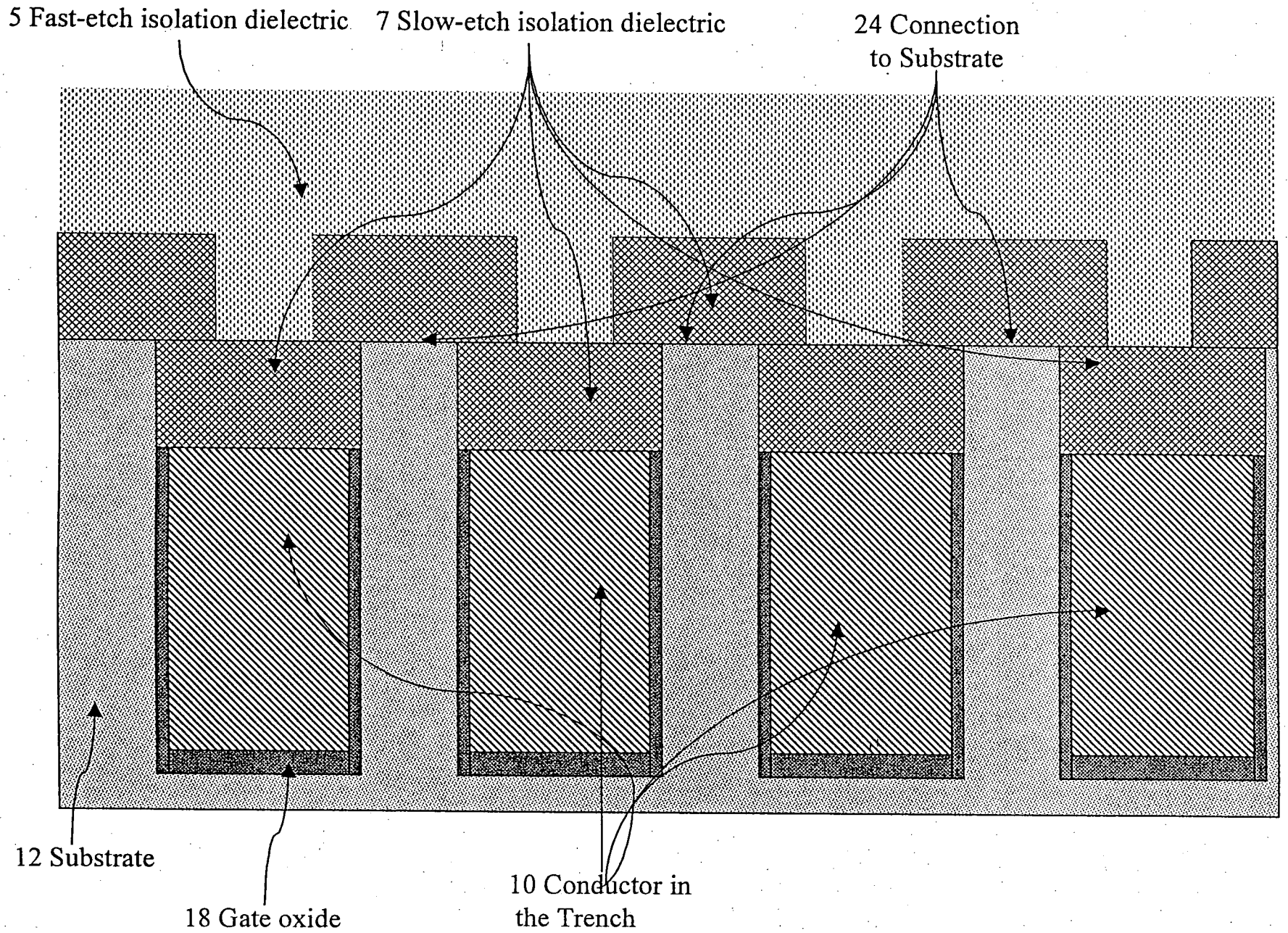
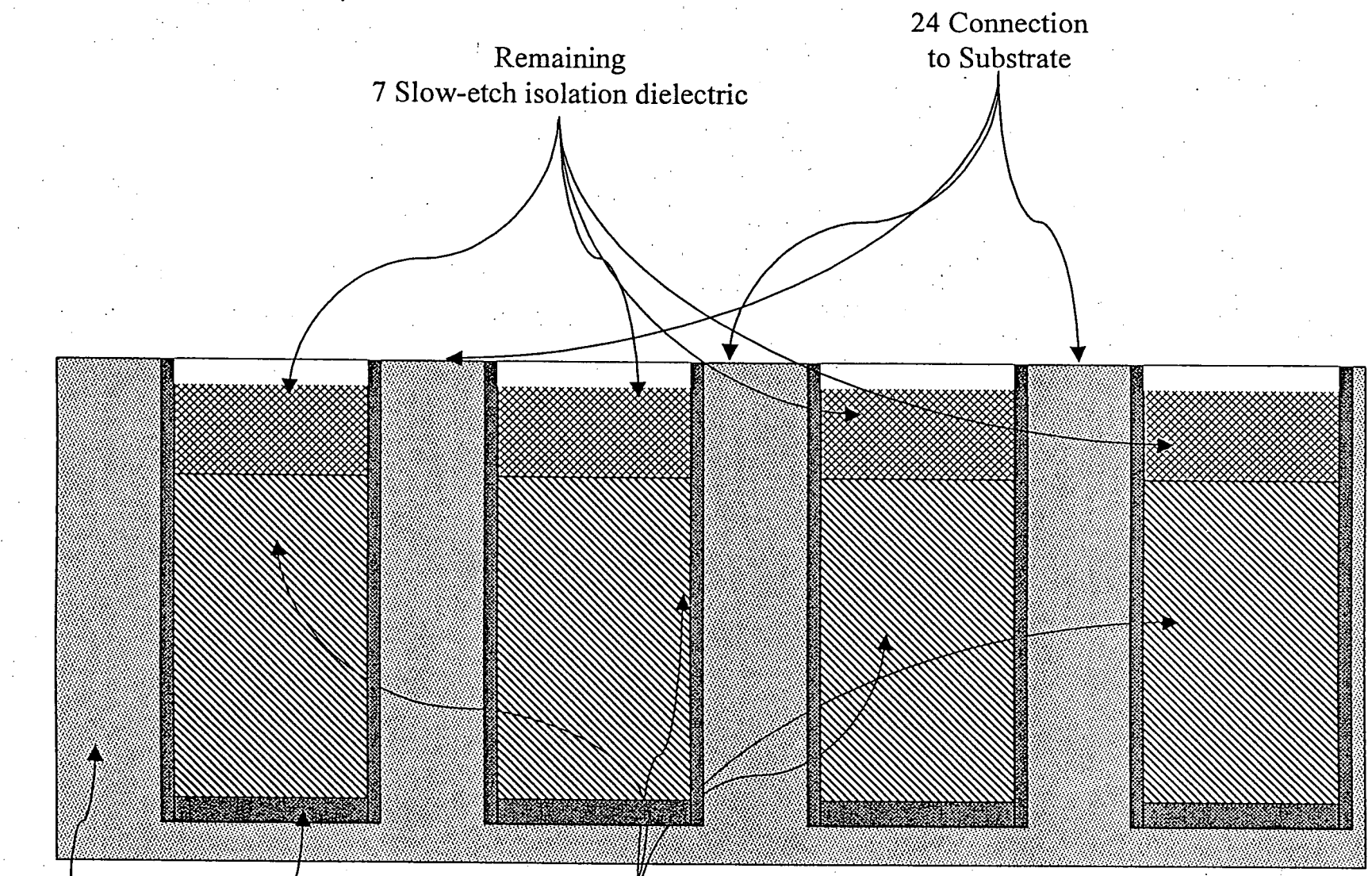


Figure 4 New Dual Isolation Dielectric after etch



Note higher density due to no alignment tolerance

Figure 5 New Dual Isolation Dielectric after etch and metal Dep.

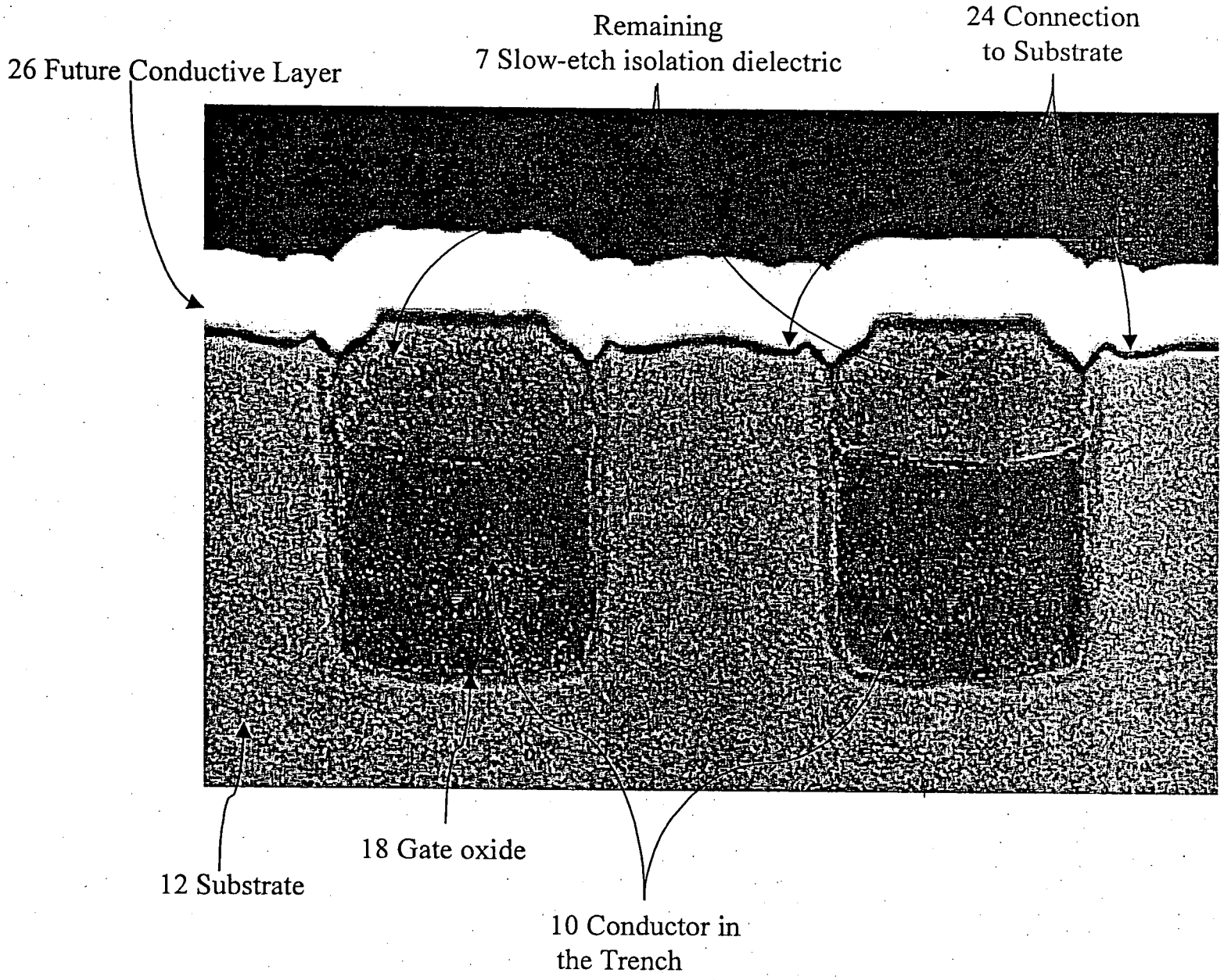


Figure 6 Isolation Dielectric after oxide growth

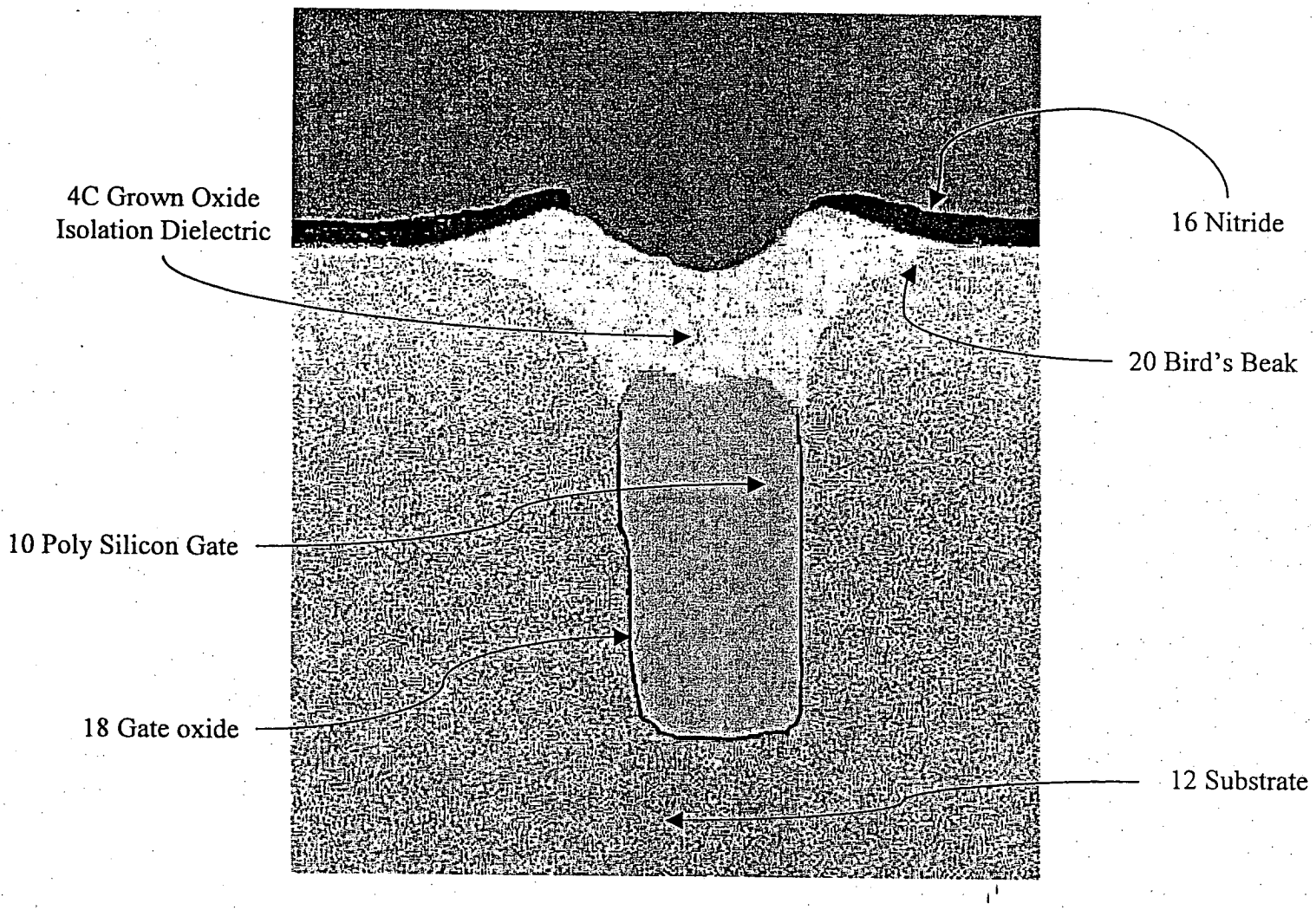


Figure 7 SOG Isolation Dielectric after Cure

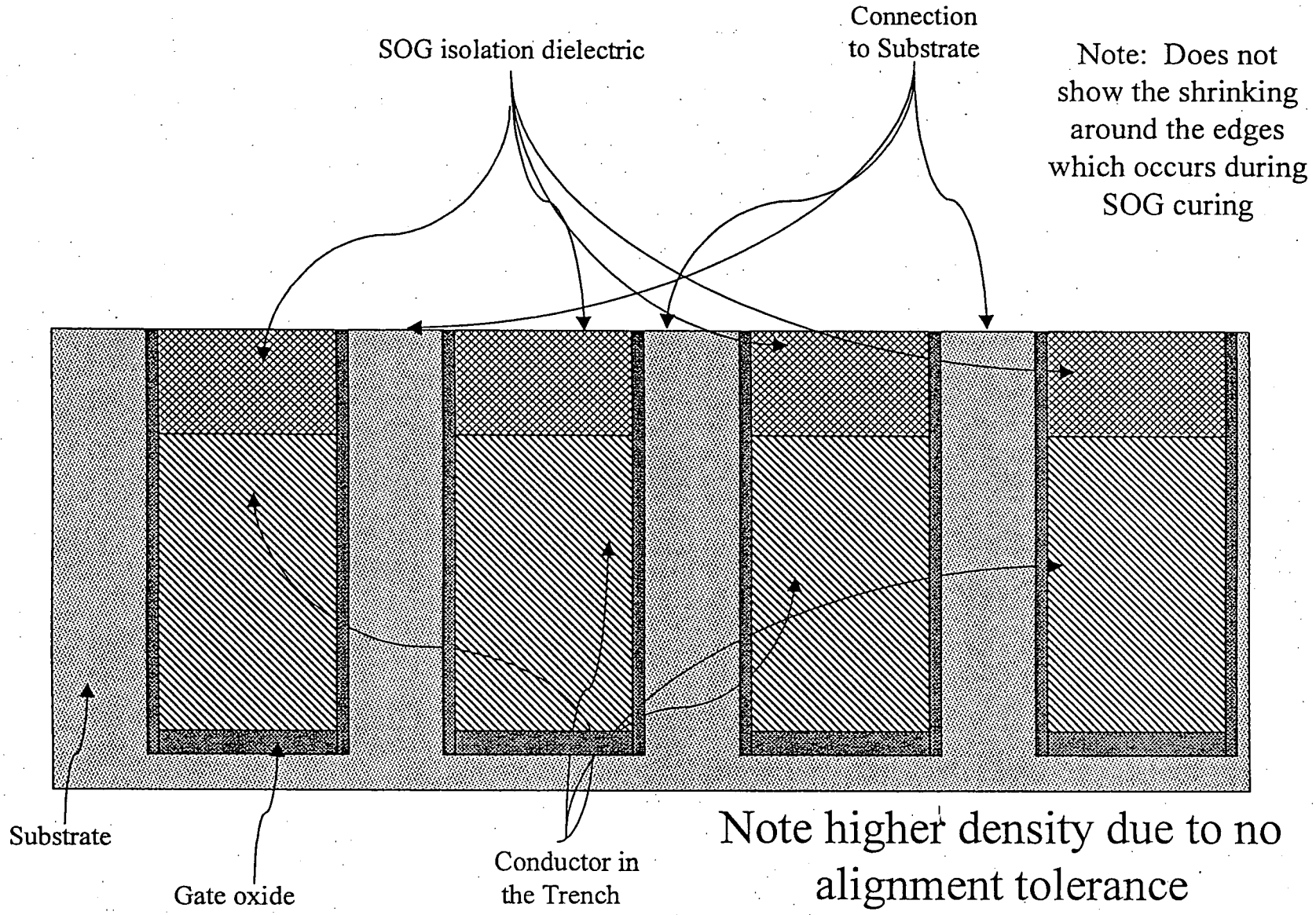
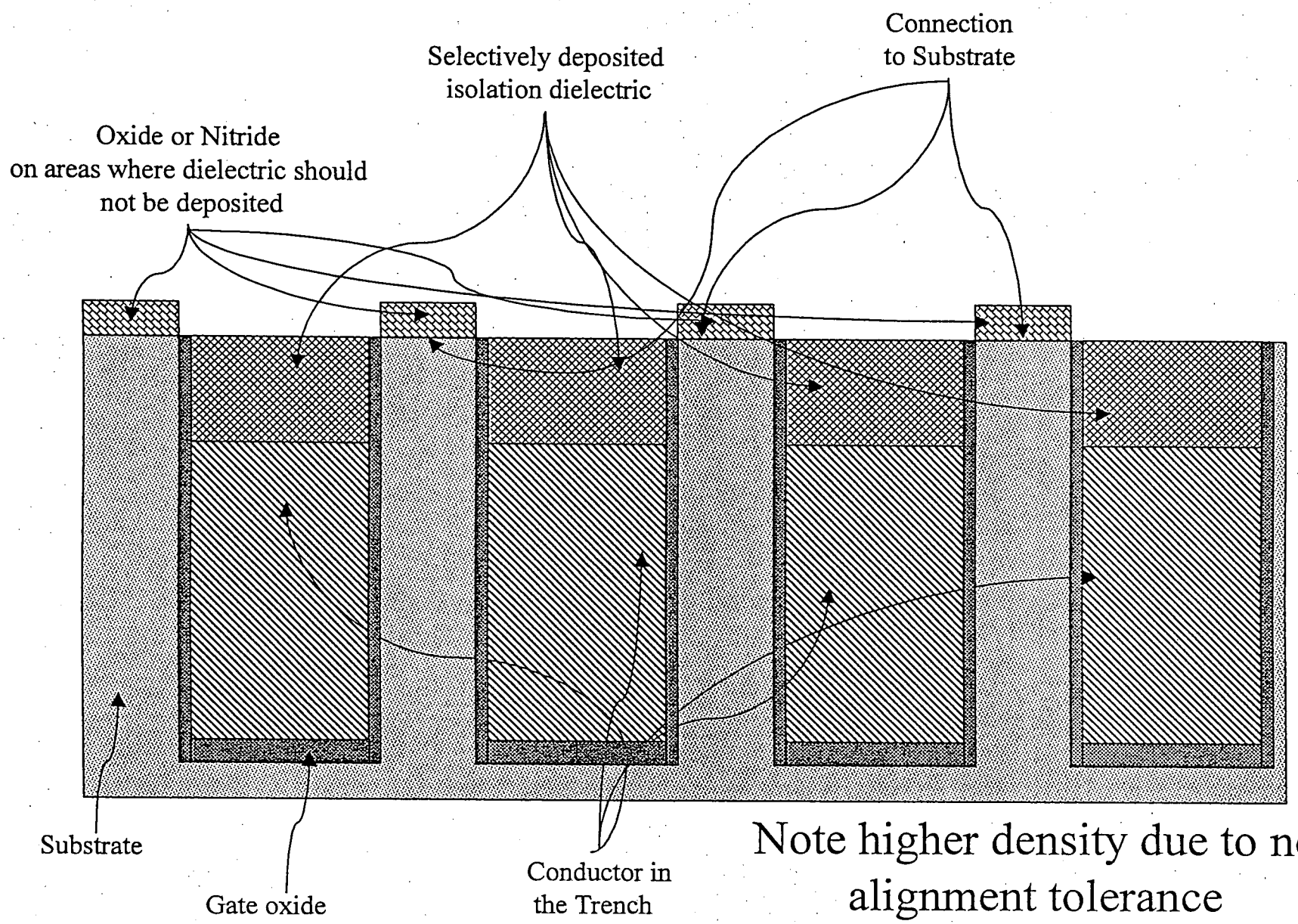


Figure 8 Selective Deposited Isolation Dielectric



Note higher density due to no alignment tolerance

Figure 9 Showing potential layout of no contact process

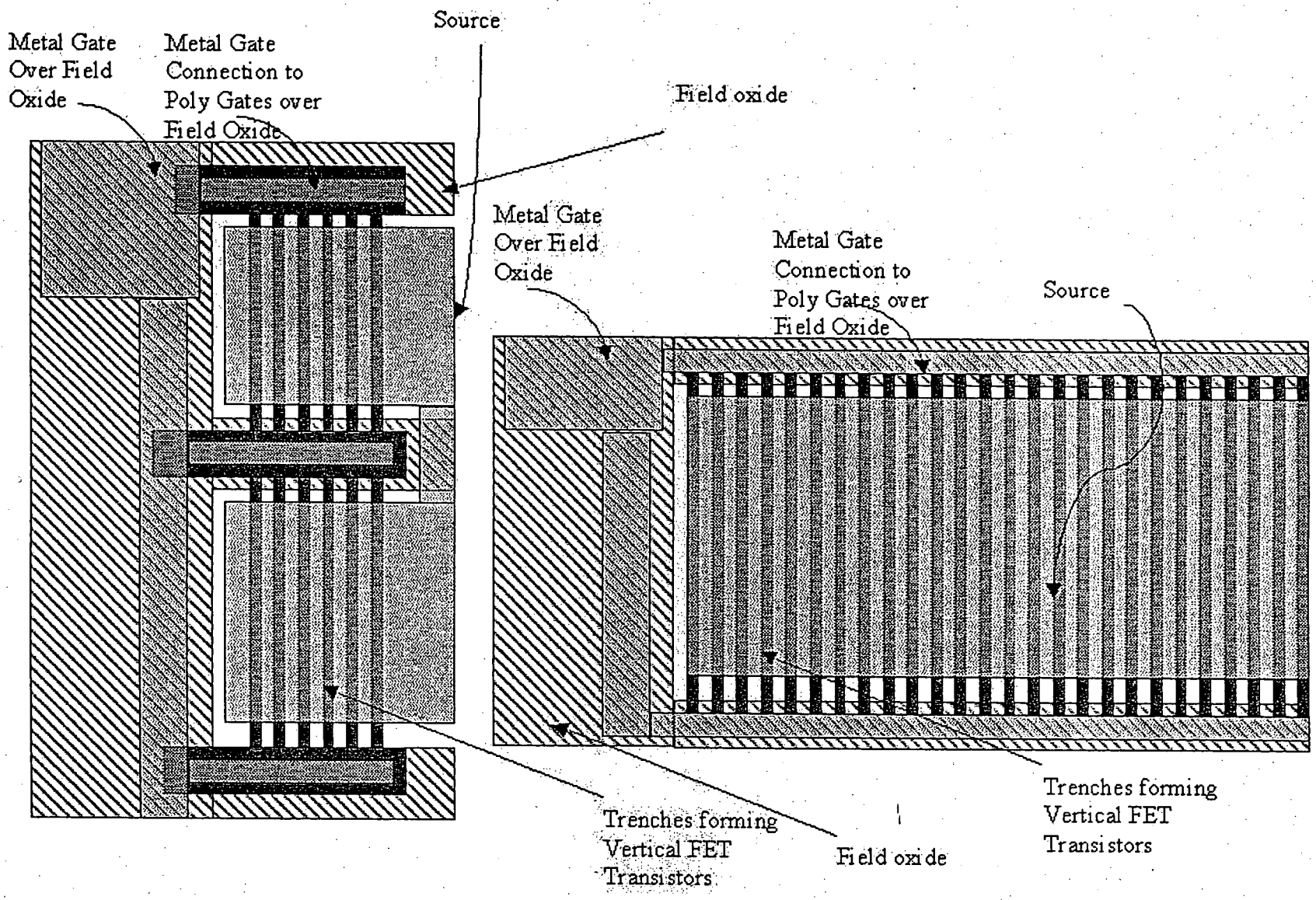


Figure 10 Showing potential layout of no contact process

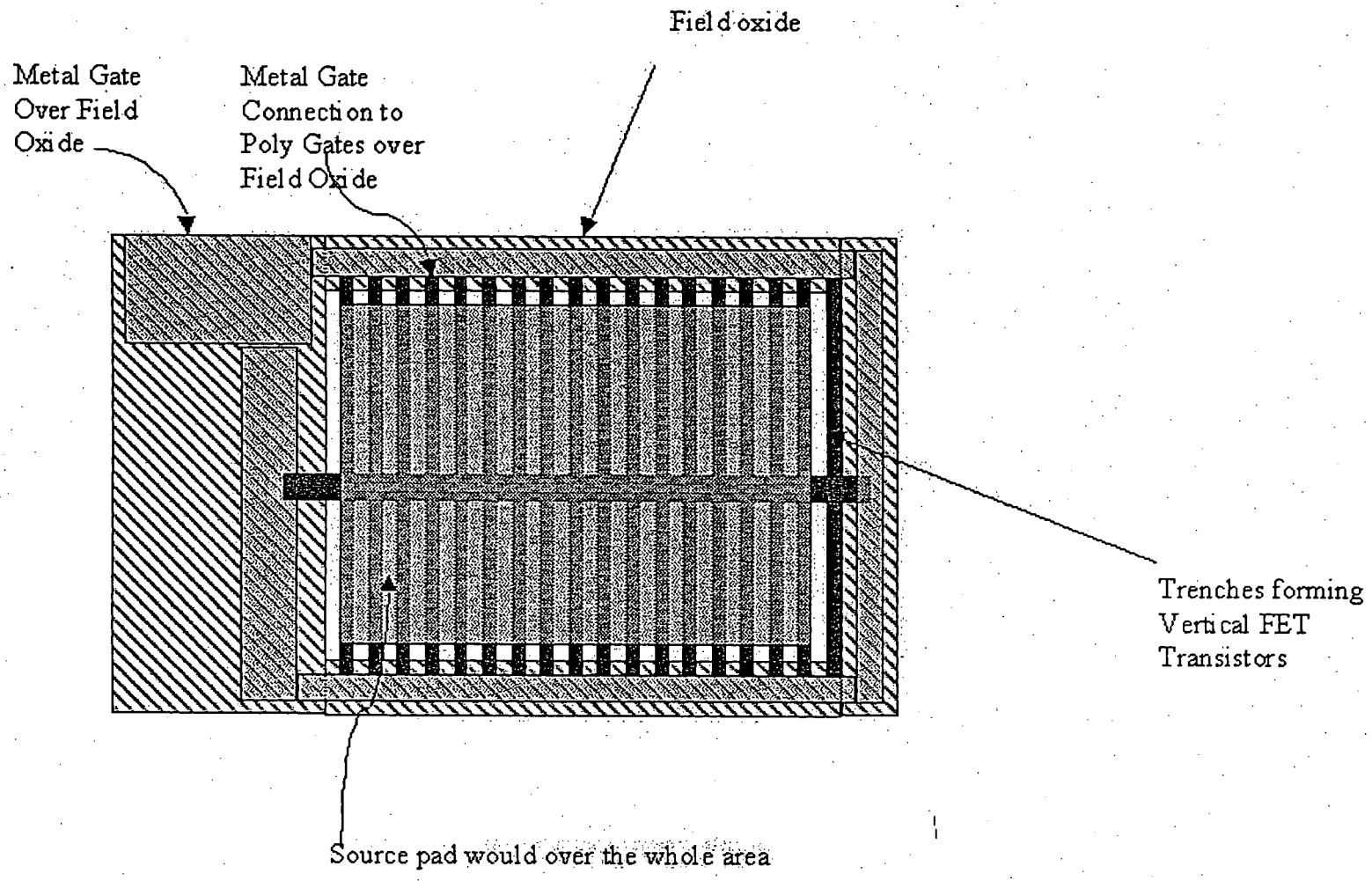


Figure 11 Showing potential layout of no contact process